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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/539,734	03/30/2000	Per Hammarlund	042390.P6873	8889

7590 07/13/2005

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EXAMINER

HUISMAN, DAVID J

ART UNIT	PAPER NUMBER
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2183

DATE MAILED: 07/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/539,734

Applicant(s)

HAMMARLUND ET AL.

Examiner

David J. Huisman

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 27 April 2005.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,2,4,6-14,18 and 20-22 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,2,4,6-14,18 and 20-22 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 30 March 2000 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-2, 4, 6-14, 16, 18, and 20-22 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: RCE and Amendment as received on 4/27/2005.

Claim Objections

3. Claim 1 is objected to because of the following informalities: Replace the phrase "retain the first microinstructions" with --retain the first microinstruction--. Appropriate correction is required.
4. Claim 8 is objected to because of the following informalities: Replace the phrase "an microinstruction source" with --a microinstruction source--. Also, replace the phrase "an microinstruction destination" with --a microinstruction destination--. Appropriate correction is required.
5. Claim 9 is objected to because of the following informalities: Replace the phrase "an microinstruction destination" with --a microinstruction destination--. Appropriate correction is required.
6. Claim 13 is objected to because of the following informalities: Remove the period before the last paragraph (before the semicolon). Appropriate correction is required.
7. Claim 21 is objected to because of the following informalities: Replace the phrase "when executed by machine" with --when executed by a machine--. Also, replace the phrase "retain the

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first microinstructions” with --retain the first microinstruction--. Appropriate correction is required.

Claim Rejections - 35 USC § 112

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. Claims 18 and 22 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

10. Claim 18 recites the limitation "The apparatus of claim 1" in line 1. There is insufficient antecedent basis for this limitation in the claim as claim 1 discloses a method and not an apparatus. It is not clear whether applicant wants claim 18 to be a method claim dependent on claim 1 or an apparatus claim dependent on claim 13. For purposes of this examination, the examiner will assume that claim 18 is dependent on claim 13.

11. Claim 22 recites the limitation "the microinstruction" in line 3. There is insufficient antecedent basis for this limitation in the claim as claim 21 discloses first and second microinstructions. Please replace "the microinstruction" with --the first microinstruction--.

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are

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such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

13. Claims 1-2, 4, 6-11, 13-14, 16, 18, and 20-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Joshi et al, U.S. Patent No. 5,954,815 (as applied in the previous Office Action and herein referred to as Joshi) in view of Schrofer, U.S. Patent No. 4,682,284 (as applied in the previous Office Action and herein referred to as Schrofer).

14. Referring to claims 1 and 21, Joshi has taught a method (and machine-readable medium for storing instructions, that when executed, perform the method) including:

a) in a queue, writing a first microinstruction of a plurality of microinstructions to a first location indicated by a write pointer. See column 4, line 51, to column 5, line 16, and note that an instruction is written to a queue. Furthermore, it is inherent that the location in the queue at which an instruction is written is governed by a write pointer. If there were no write pointer, then the system would not know which location to write to.

b) the plurality of microinstructions being written to the queue as a set of a predetermined number of microinstructions. See column 4, lines 7-11, and column 4, line 51, to column 5, line 16. Note that microinstructions are written to a queue as a set of a predetermined number of microinstructions (i.e., the number of instructions that are received by the queue is determined by how many instructions are dispatched each clock cycle, if no instructions are dispatched, then all four instructions are placed in the queue, which is known beforehand, or predetermined).

c) the first microinstruction of the plurality of microinstructions being indicated as invalid on account of being outside a macroinstruction. See column 7, lines 1-21, and note that a first microinstruction of the plurality of microinstructions would be indicated as being invalid on account of being outside a macroinstruction. More specifically, in the case where the first

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microinstruction follows a branch macroinstruction for which a branch prediction is made, it will be invalidated. It should be realized that a macroinstruction is an instruction which may be broken down into multiple sub-instructions. Consequently, from column 6, lines 45-51, a branch instruction is a macroinstruction because it is actually broken down into an initial branch instruction and a delay instruction.

d) while Joshi has taught invalidating instructions, which implies that those instructions are not to be retained in the queue, Joshi has not explicitly taught multiple limitations in claim 1.

However, Schrofer has taught the limitations which Joshi fails to teach, including:

d1) making a qualitative determination whether or not to retain the first microinstruction within the queue based on the indicated invalidity of the first microinstruction. See Schrofer, column 3, lines 10-32. It should be noted from the abstract that Schrofer's queue holds instructions which are eventually executed.

d2) if the qualitative determination is to retain the first microinstruction, then advancing the write pointer to indicate a second location within the queue into which to write a second microinstruction. See Schrofer, column 3, lines 10-32.

d3) if the qualitative determination is not to retain the first microinstruction, then maintaining the write pointer to indicate the first location within the queue into which to write the second microinstruction, so that the first microinstruction is overwritten by the second microinstruction. See Schrofer, column 3, lines 10-32.

As disclosed by Schrofer in column 2, line 62, to column 3, line 9, and column 2, lines 3-16, such a technique of dealing with invalidated instructions maximizes queue efficiency. For instance, when an instruction is invalidated in Schrofer, a next instruction will overwrite the

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invalid instruction instead of the next instruction being stored in a next free queue location after the invalid instruction. The latter technique would result in an invalidated (and useless) instruction taking up queue storage space. By overwriting an invalidated instruction, the queue would only contain valid instructions, thereby maximizing efficiency. As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Joshi to include the teachings of Schrofer so that when instructions are invalidated in Joshi, they may be overwritten instead of left to take up precious storage space within the queue.

15. Referring to claim 2, Joshi in view of Schrofer has taught a method as described in claim

1. Schrofer has further taught that the qualitative determination includes examining a valid bit associated with the first microinstruction to determine validity of the first microinstruction (Fig.4, components 310, 315, and 301, and column 11, lines 16-25), making the qualitative determination to retain the first instruction if the valid bit indicates the first instruction is being valid, and making the qualitative determination not to retain the first instruction if the valid bit indicates the first instruction as being invalid (column 3, lines 10-32).

16. Referring to claim 4, Joshi in view of Schrofer has taught a method as described in claim

2. Joshi has further taught that a plurality of microinstructions are written to the queue in a set of a predetermined number of microinstructions (column 4, lines 7-11, and column 4, line 51, to column 5, line 16; the number of instructions that are received by the queue is determined by how many instructions are dispatched each clock cycle. If no instructions are dispatched, then all four instructions are placed in the queue, which is known beforehand, or predetermined), and wherein at least one microinstruction of the set is indicated as being invalid on account of a branch misprediction relating to a branch microinstruction upstream of the at least one

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microinstruction in a stream of microinstructions (column 6 lines 35-53, and column 7, lines 1-21). Also, as is known, when branch prediction is employed, and the prediction is wrong, instructions along the wrong path must be invalidated.

17. Referring to claim 6, Joshi in view of Schrofer has taught a method as described in claim 1. Joshi has further taught that the first microinstruction is written to the queue from a microinstruction cache. See Fig.3, component 34 (instructions from cache 34 are written to queues 66).

18. Referring to claim 7, Joshi in view of Schrofer has taught a method as described in claim 6. Joshi has further taught that the first microinstruction is part of a trace of microinstructions received from the microinstruction cache. See column 4, lines 7-11, and column 4, line 51, to column 5, line 16, and note that several instructions are dispatched from the cache to the queue, as part of a trace, where a trace is merely a sequence of instructions.

19. Referring to claim 8, Joshi in view of Schrofer has taught a method as described in claim 6. Schrofer has further taught that the first microinstruction is received from a microinstruction source operating in a first clocking domain into the queue and read from the queue to a microinstruction destination operating in a second clocking domain. See column 9, line 62, to column 10, line 15. It is described here that the clock signal that writes information into the queue is at a different frequency than the clock signal that is used to read information out of the queue.

20. Referring to claim 9, Joshi in view of Schrofer has taught a method as described in claim 1. Joshi has further taught that the first microinstruction is received into the queue as part of a set of microinstructions comprising a first predetermined number of microinstructions and read

from the queue to a microinstruction destination as part of a second set of microinstructions comprising a second number of microinstructions. See column 4, lines 7-11, and column 4, line 51, to column 5, line 16, and note that the number of instructions that are received by the queue is determined by how many instructions are dispatched each clock cycle. If no instructions are dispatched, then all four instructions are placed in the queue, and since different instructions are dispatched to different execution paths (Fig.3, components 74 and 82), instructions in some paths will take longer or shorter amounts of times, depending on the path it is in, therefore being part of different sets of instructions when it enters the queue and when it leaves the queue.

21. Referring to claim 10, Joshi in view of Schrofer has taught a method as described in claim 1. Schrofer has further taught that the first microinstruction is written from a source to a destination, and wherein the queue comprises a first path between source and destination, the method including propagating the first microinstruction from the source to the destination via a second path, not including the queue, if the queue is empty. See column 3, lines 40-58.

22. Referring to claim 11, Joshi in view of Schrofer has taught a method as described in claim 10. Schrofer has further taught selecting between the first and second paths to receive the first microinstruction for propagation to the destination. See column 3, lines 40-58.

23. Referring to claim 13, Joshi has taught an apparatus comprising:

a) a queue to buffer a first microinstruction propagated from a source to a destination. See Fig.3 and column 4, line 51, to column 5, line 16.

b) the first microinstruction is written to the queue as part of a set including a predetermined number of microinstructions. See column 4, lines 7-11, and column 4, line 51, to column 5, line 16. Note that microinstructions are written to a queue as a set of a predetermined number of

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microinstructions (i.e., the number of instructions that are received by the queue is determined by how many instructions are dispatched each clock cycle, if no instructions are dispatched, then all four instructions are placed in the queue, which is known beforehand, or predetermined).

c) at least one microinstruction of the set is indicated as being invalid on account of being outside a macroinstruction. See column 7, lines 1-21, and note that a first microinstruction of the plurality of microinstructions would be indicated as being invalid on account of being outside a macroinstruction. More specifically, in the case where the first microinstruction follows a branch macroinstruction for which a branch prediction is made, it will be invalidated. It should be realized that a macroinstruction is an instruction which may be broken down into multiple sub-instructions. Consequently, from column 6, lines 45-51, a branch instruction is a macroinstruction because it is actually broken down into an initial branch instruction and a delay instruction.

d) while Joshi has taught invalidating instructions, which implies that those instructions are not to be retained in the queue, Joshi has not explicitly taught multiple limitations in claim 1.

However, Schrofer has taught the limitations which Joshi fails to teach, including write logic to:

d1) make a qualitative determination whether or not to retain the first microinstruction within the queue. See Schrofer, column 3, lines 10-32. It should be noted from the abstract that Schrofer's queue holds instructions which are eventually executed.

d2) if the qualitative determination is to retain the first microinstruction, advance a write pointer to indicate a second location within the queue into which to write a second microinstruction. See Schrofer, column 3, lines 10-32.

d3) if the qualitative determination is not to retain the first microinstruction, maintain the write pointer to indicate the first location within the queue into which to write the second microinstruction, so that the first microinstruction is overwritten by the second microinstruction. See Schrofer, column 3, lines 10-32.

As disclosed by Schrofer in column 2, line 62, to column 3, line 9, and column 2, lines 3-16, such a technique of dealing with invalidated instructions maximizes queue efficiency. For instance, when an instruction is invalidated in Schrofer, a next instruction will overwrite the invalid instruction instead of the next instruction being stored in a next free queue location after the invalid instruction. The latter technique would result in an invalidated (and useless) instruction taking up queue storage space. By overwriting an invalidated instruction, the queue would only contain valid instructions, thereby maximizing efficiency. As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Joshi to include the teachings of Schrofer so that when instructions are invalidated in Joshi, they may be overwritten instead of left to take up precious storage space within the queue.

24. Referring to claim 14, Joshi in view of Schrofer has taught an apparatus as described in claim 13. Furthermore, the apparatus of claim 14 performs the method of claim 2.

Consequently, claim 14 is rejected for the same reasons set forth in the rejection of claim 2.

25. Referring to claim 16, Joshi in view of Schrofer has taught an apparatus as described in claim 14. Furthermore, the apparatus of claim 16 performs the method of claim 4.

Consequently, claim 16 is rejected for the same reasons set forth in the rejection of claim 4.

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26. Referring to claim 18, Joshi in view of Schrofer has taught an apparatus as described in claim 13. Furthermore, the apparatus of claim 18 performs the method of claim 6.

Consequently, claim 18 is rejected for the same reasons set forth in the rejection of claim 6.

27. Referring to claim 20, Joshi in view of Schrofer has taught an apparatus as described in claim 13. Furthermore, the apparatus of claim 20 performs the method of claim 10.

Consequently, claim 20 is rejected for the same reasons set forth in the rejection of claim 10.

28. Referring to claim 22, Joshi in view of Schrofer has taught a machine-readable medium as described in claim 21. Schrofer has further taught that the sequence of microinstructions cause a multiprocessor to perform the step of examining a valid bit associated with the microinstruction to determine validity of the first microinstruction (Fig.4, components 310, 315, and 301, and column 11, lines 16-25), to make the qualitative determination to retain the first instruction if the valid bit indicates the first instruction as being valid, and to make the qualitative determination not to retain the first instruction if the valid bit indicates the first instruction as being invalid (column 3, lines 10-32).

15. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Joshi in view of Schrofer, as applied above, and further in view of Nemirovsky et al, U.S. Patent No. 6,477,562 (as applied in the previous Office Action and herein referred to as Nemirovsky).

16. Referring to claim 12, Joshi in view of Schrofer has taught a method as described in claim 1. Joshi in view of Schrofer has not taught that the queue includes a first portion to support a first thread within a multithreaded environment and a second portion to support a second thread within the multithreaded environment, and wherein the first location into which

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the first microinstruction is written is located in the first portion if the first microinstruction comprises part of the first thread. However, Nemirovsky has taught such a concept. See column 6 line 65, to column 7, line 11, and note that since a single queue could be partitioned for separate threads, it would be inherent that if one partition was allocated for a particular thread, than an instruction pertaining to that thread would be placed in that partition, or portion. Having separate portions or partitions in the queue for different threads allows the scheduler that dedicates different resources to the individual threads to easily access the instructions from the individual threads. When the scheduler is to send an instruction from thread 2, for example, it may go to the first entry from the second portion of the queue to find the next instruction for that thread, instead of searching through all the instructions for the next instruction for the second thread, which would result in a longer delay. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Joshi and Schrofer in view of Nemirovsky to have separate portions or partitions in the queue for individual threads to reduce the amount of time to find and access the next instruction to be processed from a particular thread.

Response to Arguments

29. Applicant's arguments filed on April 27, 2005, have been fully considered but they are not persuasive.

30. Applicant argues the novelty/rejection of claims 1, 12-13, and 21 on page 10 of the remarks, in substance that:

"Since Joshi fails to disclose or suggest a microinstruction or a macroinstruction, the Office action cites Mitchell to disclose a microinstruction. However, there is no indication in Joshi, Mitchell, or a combination thereof that a macroinstruction cannot comprise one or more

microinstructions preceding a delay microinstruction as well as one or more microinstructions following the same delay microinstruction. In other words, there is no indication in Joshi-Mitchell combination that a microinstruction that comes after a delay microinstruction is outside a macroinstruction. In contrast, claim 1 requires "the first microinstruction of the plurality of microinstructions being indicated as invalid on account of being outside a macroinstruction."

31. These arguments are not found persuasive for the following reasons:

a) It should be realized that a macroinstruction is an instruction that is replaced by a predefined sequence of sub-instructions (microinstructions). Joshi has taught exactly this when it comes to the branch instruction. The branch macroinstruction is actually defined by two microinstructions (the initial branch instruction and the delay instruction). Joshi does not disclose that the branch includes any additional microinstructions. If a microinstruction is not the initial branch instruction or the delay instruction, then it is outside of the branch macroinstruction. Consequently, if a microinstruction follows the delay instruction, it is not part of the branch macroinstruction. Instructions that follow and are not part of a predicted branch macroinstruction are invalidated.

Conclusion

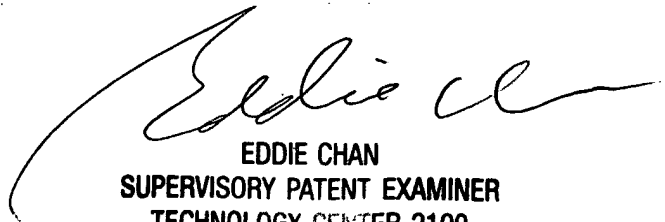
Any inquiry concerning this communication or earlier communications from the examiner should be directed to David J. Huisman whose telephone number is (571) 272-4168. The examiner can normally be reached on Monday-Friday (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DJH
David J. Huisman
July 7, 2005



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